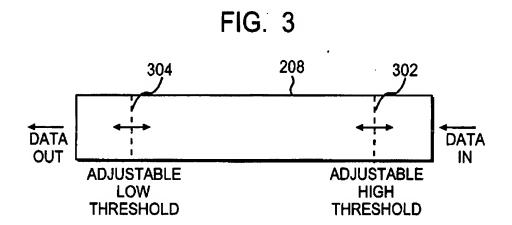
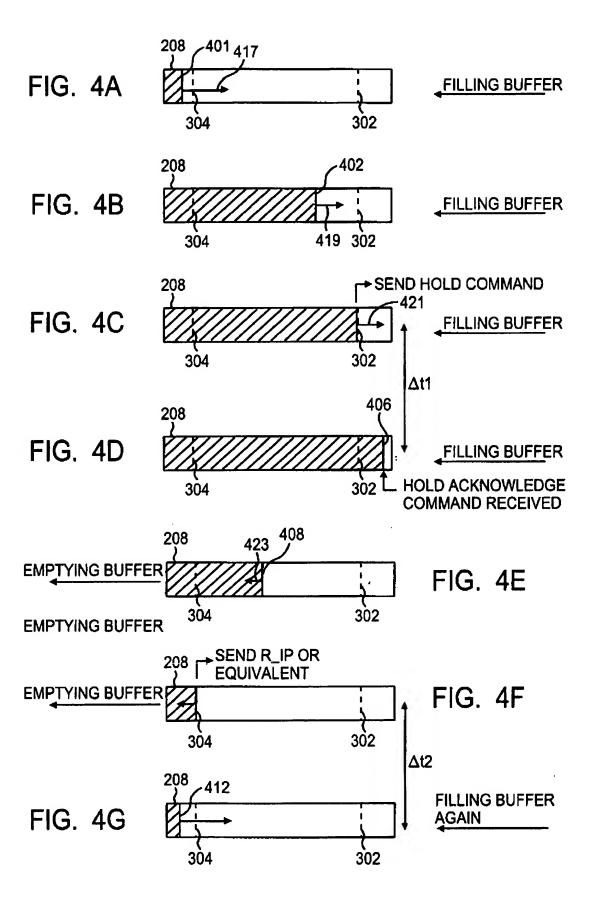


FIG. 2 140-150a 212 214 209 **PROCESSOR LINK LAYER** PHY **CIRCUITRY CIRCUITRY LAYER** 206 BUFFER CONTROL CIRCUITRY STP/SAS CONNECTION 210 208¦ **RECEIVE** DATA (**MEMORY BUFFER** DATA; IN OUT 170 172





....

FIG. 5

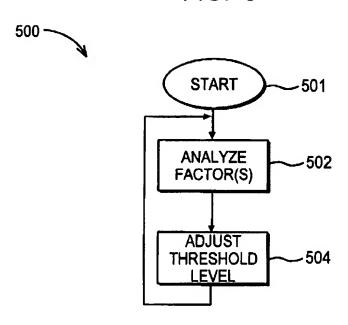
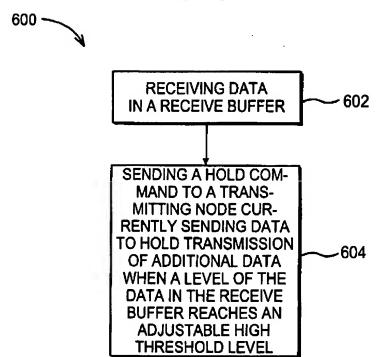


FIG. 6



•• , • • . .